

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	7043	((703/28) or (716/106,107,108,136) or (714/11)).OCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/02/15 16:22
L3	1	("5442772").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/02/15 16:25
L4	0	3 and (virtual adj microcontroller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/02/15 16:27
L5	124	((virtual emulat\$4 simulat\$5 test\$3) adj (microcontroller) and (lock\$step\$3 synchroniz\$7))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/02/15 16:38
S1	3	((("6578174") or ("7073158") or ("7024636")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2011/10/05 09:43
S2	6772	((703/28) or (716/106,107,108,136) or (714/11)).OCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2011/10/05 09:46
S3	116	((virtual emulat\$4 simulat\$5 test\$3) adj (microcontroller) and (lock\$step\$3 synchroniz\$7))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/10/05 10:52
S4	2078	((virtual emulat\$4 simulat\$5 test\$3) adj (processor) and (lock\$step\$3 synchroniz\$7))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/10/05 11:00
S5	2029	((virtual emulat\$4 simulat\$5 test\$3) adj (processor) and (lock\$step\$3 synchroniz\$7))	US-PGPUB; USPAT	OR	ON	2011/10/05 11:02
S6	627	((virtual emulat\$4 test\$3) adj (cpu) and (lock\$step\$3 synchroniz\$7))	US-PGPUB; USPAT	OR	ON	2011/10/05 11:49

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	126	((virtual emulat\$4 simulat\$5 test\$3) adj (microcontroller) and (lock\$step\$3 synchroniz\$7))	US-PGPUB; USPAT; UPAD	OR	ON	2012/02/15 16:20
S7	109	((virtual emulat\$4 simulat\$5 test\$3) adj (microcontroller) and (lock\$step\$3 synchroniz\$7))	US-PGPUB; USPAT; UPAD	OR	ON	2011/10/05 12:06
S8	12	((virtual emulat\$4 simulat\$5 test\$3) adj (microcontroller) and (lock\$step\$3 synchroniz\$7)).clm.	US-PGPUB; USPAT;	OR	ON	2011/10/05 12:06

			UPAD			
S9	36	((synchon\$7 lock\$step\$5) and (halt\$4 break\$4 stop\$4) and (cpu processor microprocessor microcontroller)).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2011/10/05 12:09
S10	13	((synchon\$7 lock\$step\$5) same (halt\$4 break\$4 stop\$4) and (cpu processor microprocessor microcontroller)).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2011/10/05 12:10
S11	10	((synchon\$7 lock\$step\$5) same (halt\$4 break\$4 stop\$4) same (cpu processor microprocessor microcontroller)).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2011/10/05 12:36
S12	8	((synchon\$7 lock\$step\$5) and (halt\$4 break\$4 stop\$4) and (cpu processor microprocessor microcontroller) and (boot\$4 initial\$7)).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2011/10/05 12:38
S13	0	((synchon\$7 lock\$step\$5) same (halt\$4 break\$4 stop\$4) same (cpu processor microprocessor microcontroller) same (boot\$4 initial\$7)).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2011/10/05 12:39

2/ 15/ 2012 4:39:41 PM
C:\ Users\ dcraig\ Documents\ EAST\ Workspaces\ 10001478_RCE_ALLOW.wsp